COUNTER MICROLOGIC® IC – A NEW DIMENSION IN MULTI-FUNCTION ELEMENTS

by George Powers

I. INTRODUCTION

One of the promises that the future holds for the system designer using integrated circuits is a selection of functional blocks that transcend the simple logic connectives which are commonplace today. Progress toward this goal reveals itself in many ways. Probably the most important indicator of the new capability for sophistication can be found in the evolution of flip-flop circuits from simple half-shift registers to complex J-K flip-flops, complete with input gate circuits, inverters, and asynchronous entry provisions. All these steps forward have been taken in a period of about two years—approximately the time since the introduction of epitaxial techniques and the improvements that were made possible as a result.

With the introduction of Counter Micrologic® integrated circuit, CμL for short, the promise of the future seems less distant than it did a few months ago. In casting about for new products to take advantage of the gains in semiconductor technology, it became apparent that more than any other single application, integrated circuits appear in various types of counters and allied functions. Here then was the next level of sophistication that would receive wide acceptance as the simpler circuits have in the past few years.

CμL compresses all of the circuit components of a printed circuit card into the space formerly occupied by a single transistor. Yet, functionally, it is equivalent to four flip-flops and at least one logic gate. CμL aims directly at the industrial market. It offers the advantages of reliability, small size, and low-power consumption at prices that are difficult to meet by most discrete component approaches and impossible by other integrated circuit approaches.

II. DESCRIPTION OF UNITS

The Counter Micrologic family originally consisted of three separate units: the CμL 958 Decade Counter, the CμL 959 Buffer Storage, and the CμL 960 Decimal Decoder. Initial enthusiasm has led to the consideration of several variations, one of which is the CμL 989 MOD 16 binary counter. The following discussion is limited to the original three and the CμL 989.

The CμL958 Decade Counter

The Fairchild CμL 958 is a monolithic decade counter designed to operate at frequencies up to 2 megacycles over a temperature range of 0°C to 75°C. Inputs consist of a count signal and a reset signal. Outputs are binary-coded decimal having 1-2-4-8 relative weighting. Individual outputs may be pulled to ground after resetting to establish any of the nine non-zero states in the normal decade sequence. Units may be cascaded to accommodate multi-digit applications.

The 958 Decade Counter consists of four flip-flops and an input amplifier as shown in Fig. 1. The flip-flops are

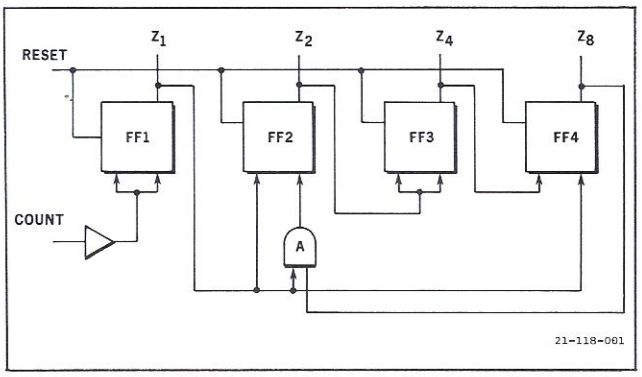

FIG. 1. CμL958 decade counter block diagram.

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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interconnected in such a way that an ordinary modulo-16 binary count is curtailed at the end of ten counts, returning to the first count rather than the eleventh. This action is accomplished by inhibiting an input to FF2 at the ninth and tenth counts, and by resetting FF4 at the end of every even-number count.

The feedback loop from FF4 to FF2 inhibits the response of FF2 to the carry pulse from FF1 during the ninth and tenth counts. At this time FF2 and FF3 are in the "zero" state and FF4 is in the "one" state. FF4 is reset at the end of counts 2, 4, 6, 8, and 10 by the signal from FF1. However, since FF4 is in the "one" state only during counts 9 and 10, only the reset after count 10 has any effect. As FF1 returns to "zero" at the end of every even-numbered pulse, the entire Counter is set to "zero" for the first count of the next cycle.

The flip-flops of the Decade Counter are similar in principle to the Fairchild μL 916 J-K flip-flop (see Fig. 2). Transistors Q_1 and Q_2 form a simple latch circuit through the cross coupling of resistors R_1 and R_2. Pulse steering transistors Q_3 and Q_4 direct a pulse of current to the base of either Q_1 or Q_2 to cause a change of the flip-flop's state. The diodes connected from the collectors of Q_1 and Q_2 to the bases of Q_3 and Q_4 select the transistor through which a count pulse may pass. Note that either Q_3 or Q_4 can be active at any particular instant, but not both, because of the complementary nature of the voltages at the collectors of Q_1 and Q_2.

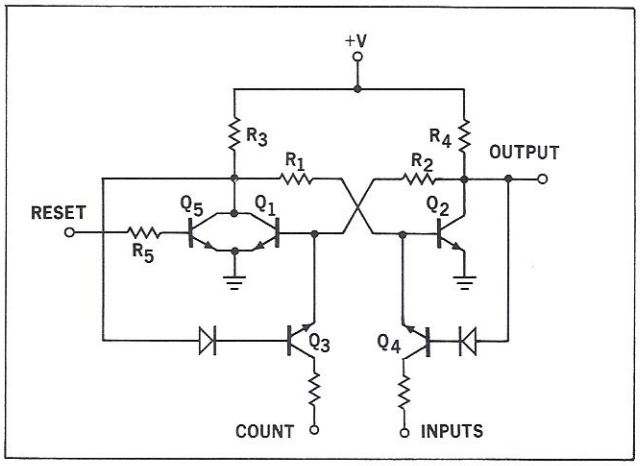

FIG. 2. Decade counter flip-flop schematic.

In FF1, FF2, and FF3, both collectors of the steering transistors are connected to the output of the previous stage (the amplifier has output characteristics similar to the flip-flop). When an output is at its low potential (less than 0.4 volt), the base-collector junction of one of the attached steering transistors is forward biased. The resulting current is responsible for a quantity of charge being present in the associated collector-base region. If the collector voltage of the pulse-steering transistors is abruptly raised (to at least 1.0 volt), the charge in the collector-base region is trapped by the diode in the base circuit. The only available exit is the emitter. The charge stored in the collector-base region exits rapidly through the emitter creating a pulse of current adequate to trigger the flip-flop exactly once.

In FF4, the collectors of the steering transistors are connected separately: one to the output of FF3, the other to the output of FF1. Thus, FF3 is responsible for setting FF4 and FF1 is responsible for clearing it. Otherwise, FF4 operates in the manner just described.

The feedback loop from FF4 output to FF2 input includes an additional transistor, which provides a discharge path from the base of Q_4 to ground when FF4 is in the "one" state. FF2 is thereby prevented from assuming the "one" state while FF4 is in the "one" state.

Each of the flip-flops contains a reset transistor, Q_5. The base resistors of all Q_5's are connected to the reset input. A reset level of at least 1.0 volts at 1.5 mA will drive all outputs to the "zero" condition (greater than 1.5 volts).

The input amplifier is non-inverting and designed to produce an output similar to that of a binary. It can also accept an output from another Decade Counter, imposing minimal loading upon it.

The CμL 989 is similar to the CμL 958 except the internal AND gate has been deleted allowing the four cascaded flip-flops to count in their natural modulus of 16. Operation at input frequencies up to 20 megacycles over the temperature range of 0°C to 75°C is possible.

The CμL959 Buffer Storage

The CμL 959 Buffer Storage unit consists of four gated latch circuits (Fig. 3) whose input characteristics match the CμL 958 Decade Counter output characteristics. The buffer storage unit serves several vital functions in a CμL system: it allows the state of the counter outputs to be sampled and held for an indefinite amount of time, it provides both true and complement signals, and it furnishes a convenient method of signal level conversion when dissimilar circuitry is to be driven.

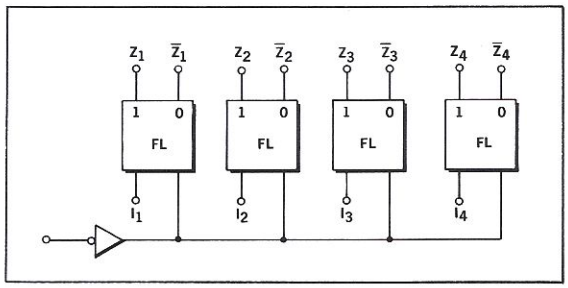

FIG. 3. CμL959 buffer storage logic diagram.

The circuit of the latch used in the CμL959 is shown in Fig. 4. Information is entered into each latch in a novel manner. The gate signal is amplified and distributed to the four latch circuits as illustrated in Fig. 3. Depending on the state of the information applied to each latch, the amplified gate signal can cause two different actions. If the information signal is high, both Q_3 and Q_4 are saturated and the base voltage at Q_1 is sufficiently low to turn Q_1 off. Transistor Q_2 starts to conduct as the collector voltage of Q_1 rises, and the latch assumes a new state. If the information input is low, Q_4 does not conduct and consequently the gate current into the base of Q_3 exits through the collector and enters the base of Q_1. Should Q_1 be off, this current turns Q_1 on, causing the latch to assume a new state. This mechanism allows a single input to satisfy both set and clear requirements in a very simple way.

The latches of the Buffer Storage unit are isolated from the load by transistors Q_5 and Q_6. These transistors will handle approximately 10 mA, and by attaching appropriate resistors externally, one may match the unit to many other circuits, both digital and analog.

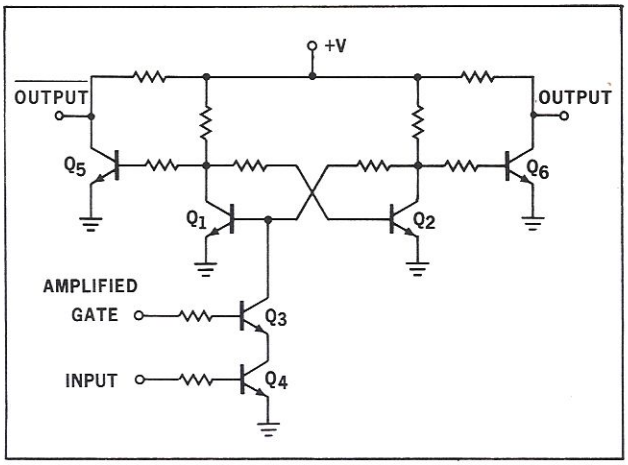

FIG. 4. Buffer storage latch circuit.

The gate amplifier is inverting, and will enable the latch inputs when low. An open gate input has the same effect. To disable the latch inputs, the gate input must be raised to 1.0 volts or more.

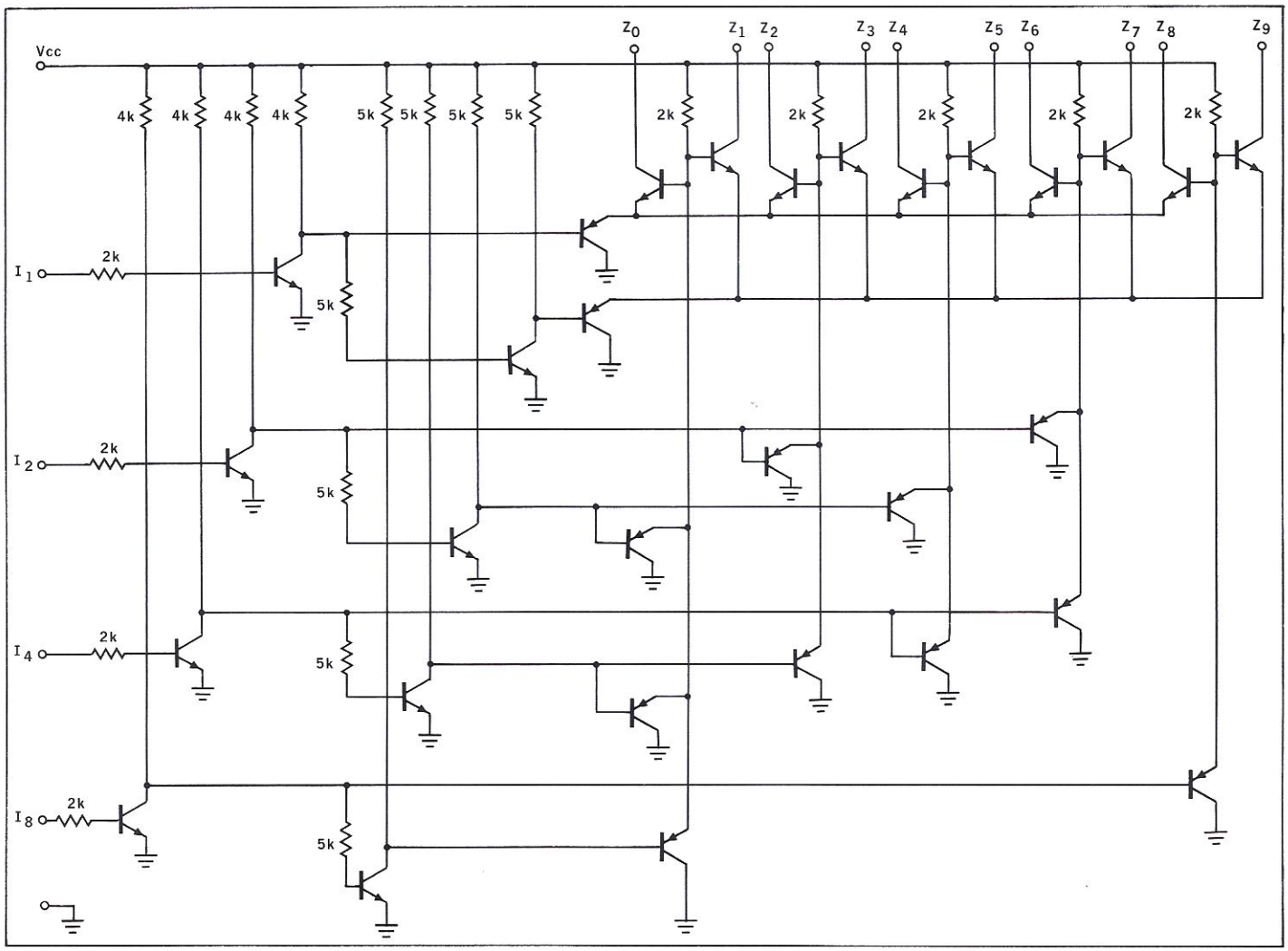

FIG. 5. CμL960 decimal decoder schematic.

The CμL960 Decimal Decoder

The unit facilitates the conversion of an 8-4-2-1 binary-coded decimal number to a true ten-digit decimal number. The input characteristics of the Decimal Decoder are adapted to the output characteristics of the CμL 958 Decade Counter. Low signal levels are accepted as logic "ones" and high signal levels as logic "zeros." As complement values are needed in the decoding matrix, and as they are not furnished by the CμL 958, inverters are included for all input signals. The outputs of the CμL 960 have voltage breakdown characteristics adequate for controlling most types of neon-filled indicator tubes.

The schematic diagram of the CμL 960 Decimal Decoder is shown in Fig. 5. The decoding matrix consists of PNP transistors used as diodes. Advantage is taken of the fact that a "one" in the most significant position never occurs unless the two successive positions are "zeros." This reduces by five the number of transistors needed in the matrix. The actual decoding process is accomplished in two steps. The first part consists of forming five new signals from the three most significant bits of the input information. One of the five signals places a positive voltage at the bases of one of five pairs of output transistors. In the second step, one of each pair is selected by the least significant input signal. The value of the least significant input signal causes a low signal at the emitters of either the even-numbered or the odd-numbered output transistors. Only one of the ten output transistors can have the proper turn-on voltages applied simultaneously to both base and emitter when a valid BCD code is used. However, because of the simplified decoding matrix, a binary code greater than nine causes two outputs to turn on simultaneously.

The output transistors can withstand voltages in excess of 60 volts and are thus quite adequate for the purpose of holding off series neon indicating devices.

III. APPLICATIONS

The CμL 958 Decade Counter can be used singly or in cascaded groups as a counter or frequency divider. The method of cascading Decade Counters is illustrated in Fig. 6. The input amplifier of each Decade Counter is non-inverting, permitting the arrangement shown. One fact should be borne in mind concerning the cascading of Decade Counters: there is a finite through delay associated with each unit of 200 nanoseconds. While the through delay is unimportant as far as any single output is concerned, it can be significant when the outputs of widely separated stages are involved. The delay manifests itself as a time difference between changing outputs—lower frequency stages lagging higher frequency stages. Through delay can be a factor in unambiguous decoding when cascaded Decade Counters are operated at speeds approaching their limit.

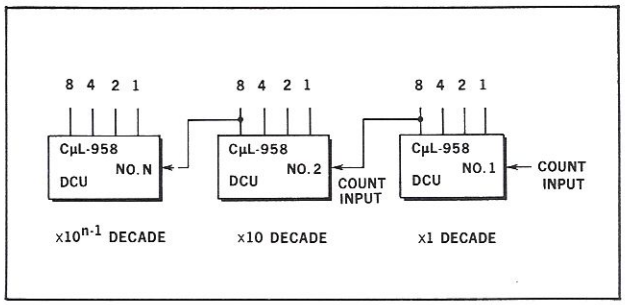

FIG. 6. Cascaded decade counter units.

Decoding

Decoding of the 958 Decade Counter with the 960 Decimal Decoder is done by simply connecting the four coded outputs of the 958 to the four corresponding 960 Decoder inputs (see Fig. 7). Each valid four-line BCD code then causes one of the ten decimal outputs to be grounded through the saturation resistance of two transistors.

In applications involving visual displays, the rate of change of the decoder outputs must be limited to accommodate the slow response of the human eye. At approximately 10 images per second, the eye loses its ability to resolve individual images. For visual display purposes, an image rate somewhat less than 10 per second must be used. This means either that a faster counter must be stopped for inspection, or that the state of the counter must be sampled and held while the counter continues. The latter method may be accomplished by interposing a CμL 959 Buffer Storage unit between the CμL 958 and CμL 960 (see Fig. 8).

The CμL 959 is in itself a very useful logic element. A subsequent application note will show a number of ways that it can be used. Among these applications are shift registers and arbitrary modulus counters.

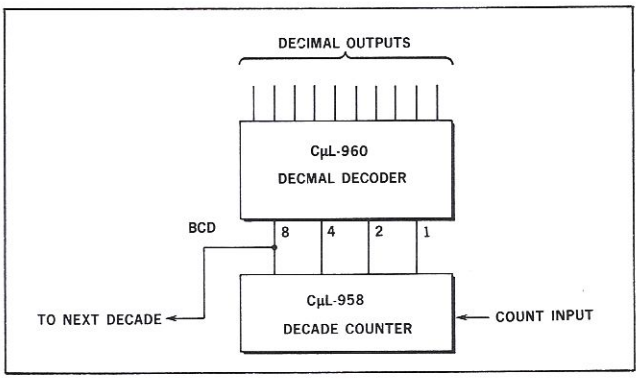

FIG. 7. Decoding the decade counter.

The gate input of the 959 Buffer Storage units affords a simple means for sampling the 958 Decade Counter. A low gate signal enables the Buffer Storage inputs and permits the

outputs to follow the information from the Decade Counter. If the gate input is now returned to the high logic level, the last state of the Decade Counter will be stored in the Buffer Storage unit and may be inspected at leisure. The duration of the gate signal and the rise and fall times of its transitron are unimportant to the storage action.

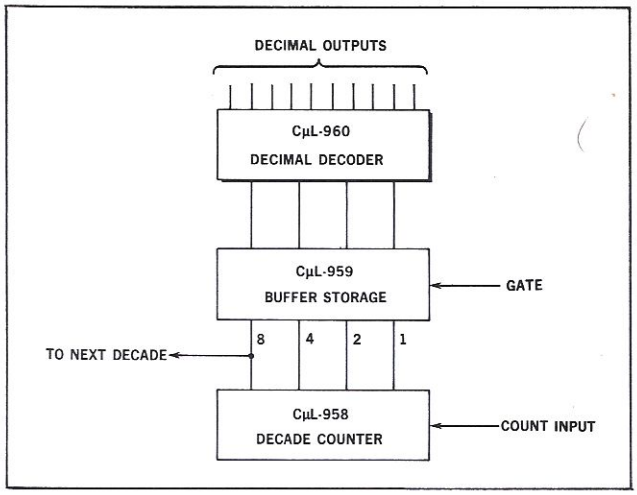

FIG. 8. Sampling the decade counter.